

AMENDMENTS**IN THE CLAIMS:**

Please amend claim 1 as follows below.

1. (Currently amended) A method for etching at least one substrate, the substrate comprising at least one silicon wafer for the fabrication of DRAM memory chips, wherein the method comprises:

a first etching step, wherein the at least one substrate is arranged for a first predetermined time in a first vessel containing a first etchant;

a first rinsing step after the first etching step, wherein the at least one substrate is arranged for a second predetermined time in a second vessel containing a first rinsing agent, the first rinsing agent containing at least one wetting agent; and

performing a second etching step after the first rinsing step while the at least one substrate is wet with the first rinsing agent containing the at least one wetting agent, wherein the at least one substrate is arranged for a third predetermined time in a third vessel containing a second etchant.

2. (Previously presented) The method according to Claim 1, wherein after the second etching step, a second rinsing step is carried out using a second rinsing agent in a fourth vessel.

3. (Previously presented) The method according to Claim 2, wherein a drying step is carried out after the second rinsing step.

4. (Previously presented) The method according to Claim 1, wherein the first etchant includes a hydrofluoric acid fraction.

5. (Previously presented) The method according to Claim 1, wherein the second etchant includes an ammonia water (NH_4OH) fraction.

6. (Previously presented) The method according to Claim 5, wherein the first rinsing agent contains the wetting agent in a concentration in the range from 0.01 to 0.1% by weight.

7. (Previously presented) The method according to Claim 1, wherein in the second etching step at least one structure with an aspect ratio in the range from 10 to 50 is introduced into the substrate.

8. (Previously presented) The method according to Claim 7, wherein the structure comprises at least one deep trench structure for a DRAM memory cell.

9. (Previously presented) The method according to Claim 1, wherein in the second etching step at least one structure with an aspect ratio of greater than 50 is introduced into the substrate.

10. (Currently amended) A method of etching a substrate, comprising:
arranging the substrate in a first vessel containing a first etchant;
performing a first etching of the substrate using the first etchant in the first vessel;
arranging the substrate in a second vessel containing a first rinsing agent comprising at least one wetting agent;
performing a first rinsing of the substrate with the first rinsing agent in the second vessel for a first predetermined time period;
while the substrate is wet with the first rinsing agent comprising the at least one wetting agent, arranging the substrate in a third vessel containing a second etchant; and
performing a second etching of the substrate using the second etchant in the third vessel for a second predetermined period of time.

11. (Previously presented) The method of Claim 10, wherein the substrate comprises a silicon semiconductor substrate.

12. (Previously presented) The method of Claim 11, wherein the silicon substrate are employed in a fabrication of DRAM memory chips.

13. (Previously presented) The method of Claim 10, further comprising performing a second rinsing of the substrate using a second rinsing agent in a fourth vessel.

14. (Previously presented) The method of Claim 13, further comprising drying the substrate after the second rinsing.

15. (Previously presented) The method of Claim 10, wherein the first etchant comprises a hydrofluoric acid fraction.

16. (Previously presented) The method of Claim 10, wherein the second etchant comprises an ammonia water (NH_4OH) fraction.

17. (Previously presented) The method of Claim 10, wherein the first rinsing agent contains the wetting agent in a concentration in the range from about 0.01% to about 0.1% by weight.

18. (Previously presented) The process according to Claim 10, wherein the second etching results in at least one structure formed within the substrate comprising an aspect ratio in the range of about 10 to about 50, wherein the at least one structure comprises at least one deep trench structure associated with a DRAM memory cell.

19. (Previously presented) The process according to Claim 10, wherein the second etching results in at least one structure formed within the substrate comprising an aspect ratio of greater than about 50.

20. (Previously presented) The process according to Claim 10, wherein the second etching results in at least one structure formed within the substrate comprising an aspect ratio in the range of about 10 to about 80.